A. Declaration

A new declaration is included herewith. The new declaration includes language directed to a single inventor, rather than joint inventors.

B. Claims 1 and 17

Claims 1 and 17 have been rejected as being obvious in view of the combination of allegedly admitted prior art, Vivio, and Sanders. A prima facie case of obviousness requires a showing that all of the claim limitations of the rejected claims are taught or suggested by the prior art. MPEP 2143 and 2143.03. An obviousness rejection is improper if all of the elements of the claim are not taught or suggested in the asserted prior art references. Applicant respectfully submits that the asserted prior art, even if taken together (the allegedly admitted prior art, Vivio, and Sanders), does not disclose or suggest the elements of claims 1 and 17.

Claim 1 is directed to a circuit, and claim 17 is directed to a method for debugging a series of microprocessor sockets configured in a serial signal path. For each microprocessor socket, if a microprocessor is present in the microprocessor socket, the microprocessor is included in the signal path. If a microprocessor is not present in a microprocessor socket, the signal path bypasses the microprocessor socket. Significant claim elements of claims 1 and 17 are not taught or suggested by any combination of the asserted prior art, whether considered alone or in combination.

First, Vivio is directed to a technique for terminating a bus in a dual processor computer system. A connector and a termination device reside at the end of the bus. When a module is inserted in the connector, the module and connector act to terminate the bus. When no module is present in the connector a termination device terminates the bus. Vivio plainly does not teach or suggest all of the claim elements of the claim 1. Vivio discloses the termination of a bus

at its free end. Vivio does not disclose the selective bypassing of empty microprocessor sockets for the sake of creating a signal path.

More specifically, Vivio does not teach or suggest the use of "plurality of microprocessor sockets adapted to form a serial signal path." Instead, the connectors of Vivio reside on a bus. Vivio does not disclose "a plurality of switches" associated with each microprocessor of the signal path. Rather, Vivio discloses a termination device that is associated with only a single processor. In addition, Vivio does not disclose the use of a switch for each of multiple processor sockets as a bypass in a signal path. In contrast, the switch device 22 of Vivio has a single purpose of terminating a bus 120 and does not teach or suggest a technique for rerouting an existing signal path around a microprocessor socket. In sum, the purpose of Vivio is to terminate a signal path, as described in the first sentence of the Vivio Abstract: "A modular computer bus providing a system for automatically maintaining proper bus termination." In direct contrast, the circuit and method of claims 1 and 17 specify the use of a continuous signal path that is made possible by switches that are operable to *bypass* signals around empty microprocessor sockets.

Second, Sanders does not disclose or suggest the claim elements of claims 1 and 17. Sanders plainly teaches that inclusion of terminator cards in empty microprocessor sockets and causing a signal to pass through the terminator cards. In Sanders, there is no teaching or suggestion of a switch that is operable to bypass signals *around* microprocessor sockets not populated by a microprocessor. It is plain that the signal in Sanders will pass through the socket regardless of whether a microprocessor is present in the microprocessor socket. In contrast, in the invention of claims 1 and 17, the signal bypasses sockets that are not populated by a microprocessor. Passing the signal through a termination card *in the socket* is not equal to

bypassing the socket. Sanders plainly provides that the terminator cards are inserted in otherwise unpopulated sockets ("Furthermore, each terminator card inserted into unpopulated Intel Slot 2 bus connectors . . . ." col. 2, lines 35-36). Because the signal of the present invention bypasses empty sockets, terminator cards are not necessary, which is one of the advantages of the present invention.

The inapplicability of Vivio and Sanders to the present invention is further demonstrated by the Examiner's attempt in the written office action to combine the teachings of Vivio and Sanders:

> It would have been obvious to a person skilled in the art at the time the invention was made to include a plurality of switches, . . . and wherein each of the switches is capable of automatically detecting whether a microprocessor is present in the corresponding microprocessor socket, . . . and if the microprocessor is not present, then the switch is automatically configured to include a *termination device* within the signal path . . . .
>
> It would have also been obvious to a person skilled in the art at the time the invention was made to modify the terminator cards taught above so that when a microprocessor is not present in the socket, a signal (e.g., JTAG signal) will still be able to pass through the *terminator card* (i.e., bypass the socket) onto the next socket, as was taught by Sanders above. . . . Further, Sanders clearly teaches that by connecting the microprocessor sockets serially with the terminator cards inserted in the empty sockets results in a more compact design and is easier to layout and route signal lines.

(Office Action, pages 5-6, emphasis added). It is instructive that the Examiner's attempt to combine the teachings of Vivio and Sanders does not result in the invention of claims 1 and 17. The Examiner's prior art combination results in the use of terminator cards in empty sockets. In plain contrast, the invention of claims 1 and 17 involves the use of switches for the purpose of bypassing empty microprocessor sockets for the sake of *avoiding* the use of termination cards in

empty microprocessor sockets. The asserted prior art plainly does not teach or suggest the invention of claims 1 and 17.

Applicant respectfully submits that the Examiner has not established a prima facie case of obviousness. The rejection of claims 1 and 17 on obviousness grounds should be withdrawn and these claims should be passed to issuance.

C. Section 112 Rejections

Claims 1, 5, and 17 have been amended to more distinctly claim the subject matter of the invention. Applicant respectfully submits that the rejection of these claims under 35 U.S.C. § 112, second paragraph should be withdrawn and these claims should be passed to issuance.

D. Claims 2-10 and 18-22

Claims 2-10 and 18-22 will not be discussed individually as each of these claims depends, either directly or indirectly, from an otherwise allowable base claim. Applicant respectfully submits that the rejection of these claims under 35 U.S.C. § 103 should be withdrawn and these claims should be passed to issuance.

Conclusion

Applicant respectfully submits that pending claims 1-10 and 17-22 of the present invention, as amended, are allowable. Applicant respectfully requests that the rejection of these claims be withdrawn and that these claims be passed to issuance.

Respectfully submitted,

Roger Fulghum
Registration No. 39,678

Baker Botts L.L.P.
910 Louisiana
One Shell Plaza
Houston, Texas 77002-4995
(713) 229-1707

Baker Botts Docket Number: 016295.0620

Date: January 16, 2004